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Paper 8
Entered: September 23, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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KINETIC TECHNOLOGIES, INC.,
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.,
Patent Owner.

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Case IPR2014-00529
Patent 7,921,320 B2

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Before GLENN J. PERRY, SCOTT A. DANIELS, and BARRY L. GROSSMAN, *Administrative Patent Judges.*

GROSSMAN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
*37 C.F.R. § 42.108*

# I. INTRODUCTION

Kinetic Technologies, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 13–24 and 37–47 of U.S. Patent No. 7,921,320 B2 (Ex. 1001, "the '320 patent"). Paper 1 ("Pet."). Skyworks Solutions, Inc., ("Patent Owner"), filed a Preliminary Response. Paper 6 ("Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314.

We determine that the information presented does not show that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of any of claims 13–24 and 37–47. Accordingly, we deny the Petition and do not institute an *inter partes* review of the '320 patent.

## *A. Related Proceedings*

Petitioner informs us of the following related matters.

The '320 Patent is at issue in *Skyworks Solutions, Inc. v. Kinetic Technologies, Inc.*, Case No. 1:13-cv-10655 (N.D. Cal.), filed March 20, 2013; and *Skyworks Solutions, Inc. v. Kinetic Technologies, Inc.*, Case No. 3:14-cv-00010 (N.D. Cal.), filed January 2, 2014.

The '320 Patent is a continuation of U.S. Application 10/144,333, now U.S. Patent No. 7,127,631, which is the subject of Reexamination Control No. 95/000,501. U.S. Patent No. 7,127,631 is at issue in *Advanced Analogic Technologies, Inc. v. Kinetic Technologies, Inc.*, Case No. 3:09-cv-01360 (N.D. Cal.), filed March 2, 2009.

U.S. Application 14/028,365, filed September 16, 2013, claims priority to the '320 Patent.

Petitioner filed a second petition (IPR2014-00530) requesting *inter partes* review of claims 13–22 and 37–45[1] of the '320 patent on grounds different from the grounds asserted in this case.

We also are aware that U.S. Patent No. 8,539,275 B2, a continuation of Application No. 11/582,927, now the '320 Patent, is the subject of a petition to institute an *inter partes* review (IPR2014-00690).

*B. The '320 Patent*

The '320 patent, titled "Single Wire Serial Interface," relates generally to control interfaces for integrated circuits ("ICs") and other devices. Ex. 1001, col. 1, ll. 14–15. The device disclosed in the '320 patent provides a single wire serial interface that may be used to control stand-alone power ICs and other devices. *Id.* at col. 1, ll. 62–64. When so used, an IC is configured to include a sensing circuit, a counter, and a ROM or similar decoder. *Id.* at col. 1, ll. 64–66.

The '320 patent describes that stand-alone power systems for power integrated circuits often are constrained by package size and cost, and where most of the available pins in such stand-alone power applications are used for power load, there are few pins in the interface left to accommodate power control functions. *Id*. at col. 1, ll. 34–43. The '320 patent states that ideally in such applications, minimal pins, or a single pin "interface would be able to accommodate a wide variety of control needs and be scalable to many levels of complexity." *Id*. at col. 1, ll. 52–58.

Figure 2 of the '320 patent, reproduced below, illustrates integrated circuit 200, which has a single wire serial interface. *Id.* at col. 2, ll. 59–60. According to the '320 patent, to use a single wire serial protocol compatible devices must provide a single wire serial interface. *Id.* at col. 3, ll. 57–60. Figure

[1] The second petition does not include a request to review claims 23, 24, 46, and 47, which are challenged in this proceeding.

2 shows a block diagram of an IC configured to provide a single wire serial interface. *Id.*

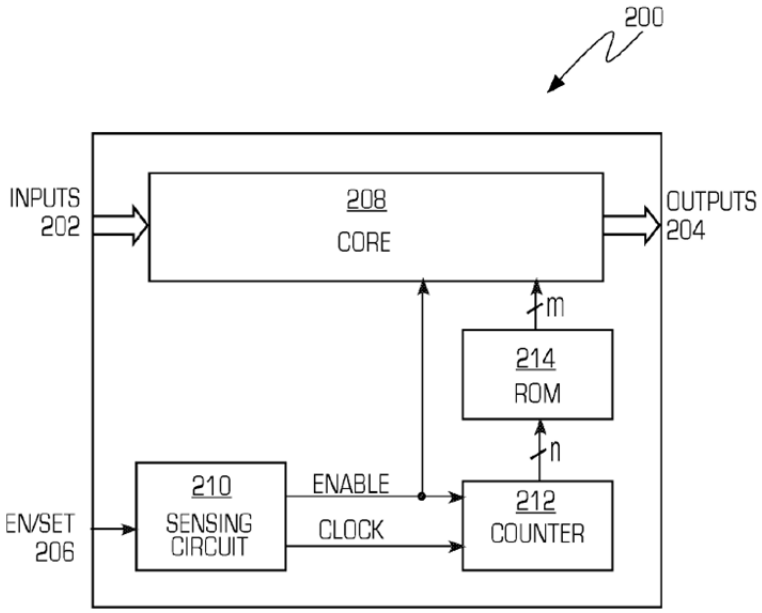


FIG. 2

As depicted in Figure 2 of the ’320 patent, integrated circuit 200 has one or more inputs 202, and one or more outputs 204, as well as EN/SET signal input 206. EN/SET input 206 is connected to sensing circuit 210, which, as discussed further below, determines the voltage state, i.e. high, low, or toggling, of the EN/SET signal. *Id.* at col. 3, l. 60–col. 4, l. 1.

Figure 1 of the ’320 patent illustrates three waveform types defining EN/SET signal. The first of these is a toggling waveform, where the EN/SET signal is composed of a series of clock pulses. The second waveform is where the EN/SET signal has a constant high value. The third waveform is where the EN/SET signal has a constant low value. Ex. 1001, col. 3, ll. 27–34.

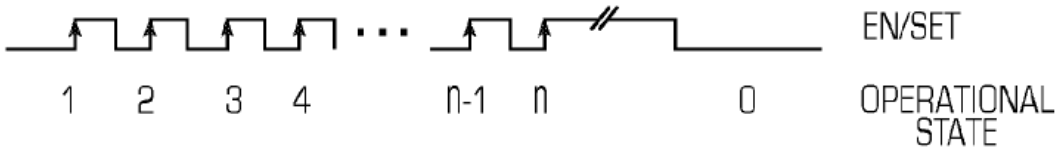


FIG. 1

The toggling waveform causes compatible devices to select particular operational states. The total number of clock pulses (or rising edges) determines the particular operational state that will be selected (i.e., four clock pulses selects the fourth operational state and so on. *Id.* at col. 3, ll. 35–39. The constant high waveform causes compatible devices to maintain their previously selected operational states. *Id.* at col. 3, ll. 43–44. The constant low waveform causes compatible devices to power off (or otherwise adopt a predefined configuration) after a pre-defined timeout period has elapsed. *Id.* at col. 3, ll. 47–49.

Sensing circuit 210 determines the waveform type of the EN/SET signal and produces two output signals, Clock signal and Enable signal, to send to counter 212. *Id*. at col. 4, ll. 1–3. The '320 patent states that:

> a rising transition of the EN/SET signal causes sensing circuit 210 to assert the Enable signal. Sensing circuit 210 holds the Enable signal high until the EN/SET signal transitions to a logical low state and remains in the low state until the predetermined timeout period has elapsed.

*Id*. at col. 4, ll. 10–15. In other words, the Enable signal is a gate signal for the Clock signal; as long as the Enable signal is high, the Clock signal is forwarded by sensing circuit 210 to counter 212. *Id*. at col. 4, ll. 15–18. In this case, counter 212 counts the transitions, i.e., waveform pulses, forwarded by sensing circuit 210 (e.g. 1, 2, 3, 4. . . n), to determine a counter n-bit output. *Id*. at col. 4, ll. 22-23. Counter 212 resets to 0 "when sensing circuit transitions the Enable signal to a low value." *Id*. at col. 4, ll. 21–25.

Devices that implement a single wire serial interface as disclosed in the '320 patent select a new control state each time a rising edge of a clock pulse is received. *Id.* at col. 4, ll. 65–67. One result is that compatible devices progressively select each control state in sequence until the desired control state is reached. *Id.* at col. 4, l. 67–col. 5, l. 2. Accordingly, selecting the eighth control state means that compatible devices will progressively select control states one through seven before finally selecting the eighth (desired) control state. *Id.* at col. 5, ll. 2–5.

### *C. Illustrative Claim*

Of the challenged claims, claims 13 and 37 are independent claims. Claim 13 is illustrative of the claimed subject matter and is reproduced below.

> 13. A power integrated circuit device having at least one input and at least one output, comprising:
>
> a core circuit producing at least one output from the power integrated circuit; and an interface for controlling the core circuit, the interface including,
>
> a first circuit for receiving a signal via a single input of the integrated circuit, the first circuit for accumulating a count of clock pulses encoded in the received signal;
>
> a second circuit for mapping the count of encoded clock pulses into a corresponding one of a plurality of control states for the core circuit;
>
> a third circuit for resetting the count of encoded clock pulses to zero in response to the received signal being low for a period that exceeds a predetermined timeout value, the predetermined timeout value being longer than a width of one of the encoded clock pulses;
>
> the first circuit outputs progressively increasing count values during the accumulating of the count of clock pulses encoded in the received signal; and
>
> the second circuit is responsive to the count values, and operative to progressively map each of the count values output during the accumulating to a corresponding one of a plurality of intermediate control states.

*D. References Relied Upon*

Petitioner relies upon the following prior art references:

| Reference | Pat./Ref. Number | Date | Exhibit Number |
|---|---|---|---|
| Loke | US 2002/0039891 Al | Apr. 4, 2002 | Ex. 1002 |
| Adlhoch | US 3,387,270 | Jun. 4, 1968 | Ex. 1003 |
| Enomoto | US 5,277,497 | Jan. 11, 1994 | Ex. 1004 |

*E. The Asserted Grounds*

Petitioner asserts that all the challenged claims, claims 13–24 and 37–47, would have been obvious under 35 U.S.C. § 103 based on Loke, combined with Adlhoch and Enomoto. Pet. 9.

## II. ANALYSIS

*A. Claim Construction*

In an *inter partes* review, "[a] claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b); *see Office Patent Trial Practice Guide*, 77 Fed. Reg. 48,756, 48,764, 48,766 (Aug. 14, 2012) (Claim Construction).

Petitioner proposes a specific construction for the phrase "receiving a signal via a single input" in independent claims 13 and 37. Pet. 7–8. Petitioner asserts that this phrase should be construed as "receiving a signal encoded with clock pulses, which signal is the same signal encoding a low period that exceeds a predetermined timeout value." *Id.* Petitioner argues that the proposed claim interpretation is required based on arguments in the prosecution history to overcome a claim rejection. *Id.* (purporting to cite "Ex. 1011 at p. 288").[2]

[2] There is no Exhibit 1011 in this case. Exhibit 1007 in this case includes the prosecution history of the '320 patent, which we assume, for purposes of this

Patent Owner asserts that Petitioner's proposed construction of the claim phrase "receiving a signal via a single input" "is incorrect because it goes beyond the broadest reasonable interpretation of the phrase." Pet. 21–22. According to Petitioner, the broadest reasonable interpretation of the phrase "is, simply, that the signal is received 'via a single input.' Thus, no construction of 'receiving a signal via a single input' is required." *Id.* at 22.

For purposes of this decision, we agree with Patent Owner. Petitioner's proposed claim construction unduly limits the broadest reasonable interpretation of the phrase "receiving a signal via a single input."

*B. Asserted Ground of Unpatentability*

Petitioner asserts that all the challenged claims would have been obvious under 35 U.S.C. § 103 based on Loke, combined with Adlhoch and Enomoto. Pet. 9.

*1. A First Circuit*

Independent claims 13 and 37 each require a first circuit for receiving a signal via a single input of the integrated circuit, and for accumulating a count of clock pulses encoded in the received signal. Ex. 1001, col. 8, ll. 59–61; col. 11, ll. 27–29. Claims 13 and 37 also each require that the output of the first circuit progressively is increasing count values when accumulating the count of clock pulses encoded in the received signal. *Id.* at col. 9, ll. 3–5; col. 11, ll. 43–45.

*a. Loke*

Petitioner asserts that pulse counter 30 in Loke corresponds to the claimed "first circuit." Pet. 10, 35. Loke discloses an amplifier control circuit particularly adapted for use in a wireless communications device, such as a mobile phone. Ex. 1002 ¶ 0008, 0010. The objective of the circuit in Loke is to reduce power usage.

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Decision, Petitioner intended to cite.

*Id.* at ¶ 0006. Loke discloses a wireless communications device that uses an amplifier module configured to amplify a radio frequency signal with increased efficiency. *Id.* at ¶ 0013. The amplifier module receives a control signal comprising a plurality of pulses. *Id.* The number of pulses within a predetermined time identifies a desired power level. *Id.*

Pulse counter 30, which Petitioner asserts corresponds to the claimed "first circuit," receives a pulse duration modulated ("PDM") signal. Ex. 1002 ¶ 62. Pulse counter 30 is an integrated circuit, which counts the pulses within the count period. *Id.* Pulse counter 30 outputs a digital number that corresponds to power output. *Id.*

Pulse counter 30 is connected to input 44 of control module 18 and to storage locations 32, 34. Ex. 1002 ¶ 63. Storage location 32 is further connected to digital-to-analog ("D/A") converter 36. *Id.* Converter 36 is connected to voltage converter 40, which in one embodiment is a DC-DC converter having output 46 for the control signal VCC. *Id.* Storage location 34 is connected to D/A converter 38, which in one embodiment is a DC-DC converter with output 48 for the control signal BIAS. *Id.* Control module 18 is shown in Figure 5 of Loke, reproduced below.

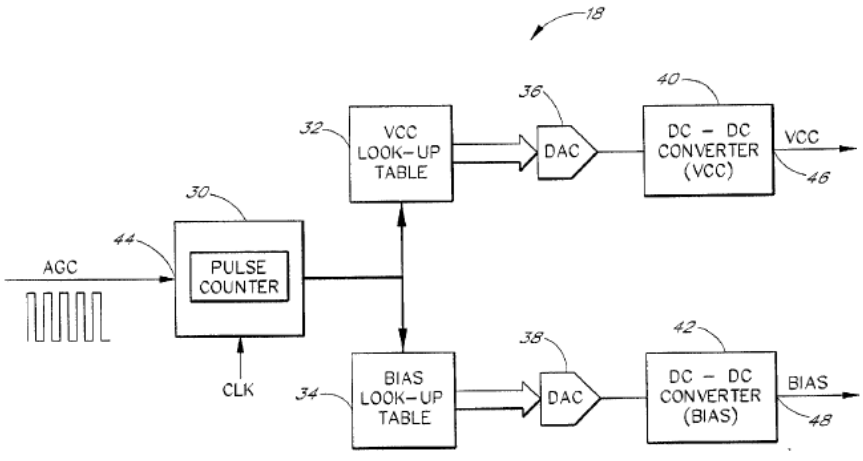


Figure 5 of Loke depicts control module 18

Petitioner acknowledges that Loke does not explicitly teach the first circuit outputting "progressively increasing count values during the accumulating of the count of clock pulses." Pet. 15, 39. Petitioner relies on Enomoto for the disclosure of this claim limitation. *Id.* According to Petitioner, counter 66 in Enomoto is a first circuit that successively counts counted values 0-831, which could be modified to send to the D/A converter in Enomoto. Pet. 15 (citing Ex. 1004, col. 7, ll. 19–21).

*b. Enomoto*

Enomoto relates to a voltage to pulse-width conversion circuit, and in particular to a voltage to pulse-width conversion circuit for adjusting the brightness of an electronic display device. Ex. 1004, col. 1, ll. 13–16. Figure 1 of Enomoto is reproduced below.

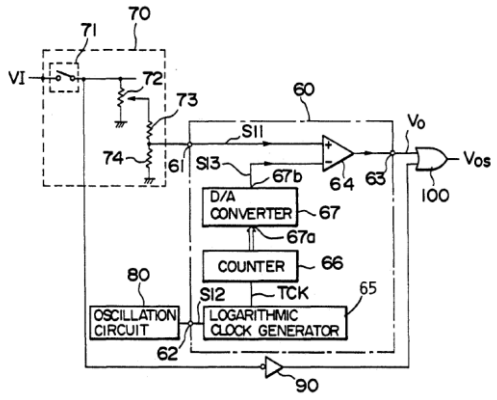


Figure 1 of Enomoto

As shown in Figure 1 of Enomoto, reproduced above, voltage to pulse-width conversion circuit 60 provides pulse width modulated ("PWM") output signal Vo for adjusting the brightness of an electronic display device, such as a display installed in a car. Ex. 1004, col. 4, ll. 64–67. Conversion circuit 60 includes voltage comparator 64, logarithmic clock generator 65, counter 66, and D/A converter 67. *Id.* at col. 5, ll. 7–9. Conversion circuit 60 also is provided with an input terminal 61 for inputting the PWM control voltage S11, input terminal 62 for

inputting a reference frequency signal S12, and output terminal 63 for outputting the PWM output signal Vo. *Id.* at col. 5, ll. 10–14. Input circuit 70 has switch 71 for lighting up, for example, instruments on the dashboard of a car. *Id.* at col. 5, ll. 33–35.

A circuit diagram of logarithmic clock generator 65 is shown in Figure 2 of Enomoto, reproduced below.

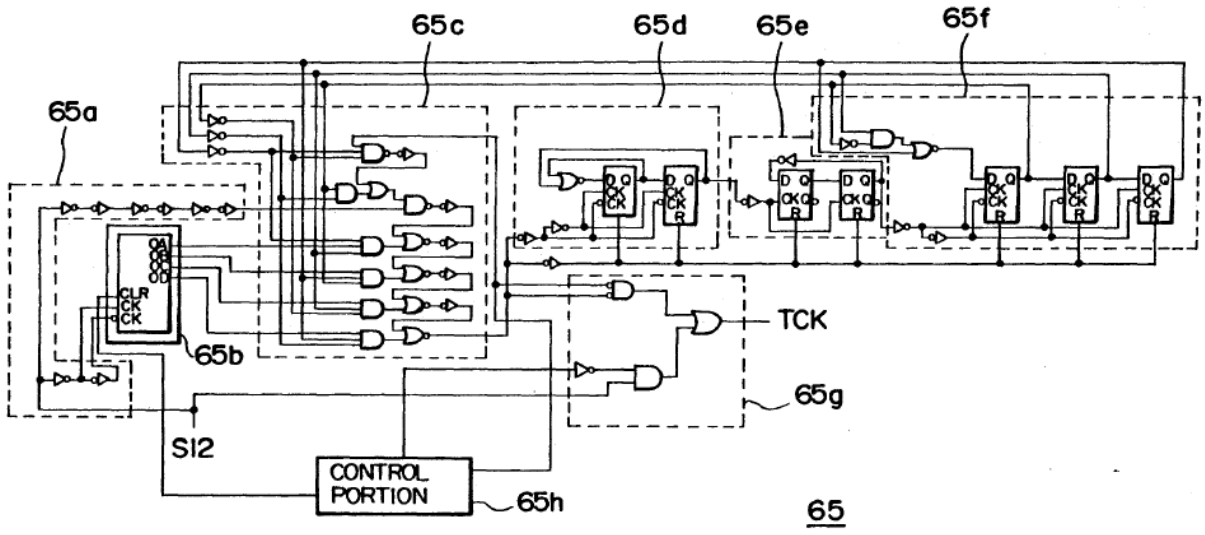


Figure 2 of Enomoto

As shown in Figure 2, logarithmic clock generator 65 includes input portion 65a, which inputs the reference frequency signal S12 and delays the signal for a predetermined time. Ex. 1004, col. 5, ll. 56–59. Clock generator 65 also includes a four-bit binary counter 65b. *Id.* at col. 5, ll. 59–60. Binary counter 65b divides the frequency of the reference frequency signal S12 by 2, 4, 8, and 16. *Id.* at col. 5, ll. 63–64. Clock selection portion 65c selects one of the outputs of the counter 65b. *Id.* at col. 5, ll. 65–66. Outputs of the clock selection portions 65c also are connected to an output portion 65g, which outputs the logarithmic clock signal TCK. *Id.* at col. 6, ll. 8–11.

When power is supplied to the circuit in Enomoto (*see* Figure 1 above),

oscillation circuit 80 oscillates and outputs reference frequency signal S12 to logarithmic clock generator 65. Ex. 1004, col. 6, ll. 58–61. Logarithmic clock generator 65 outputs reference frequency signal S12 to counter 65b through input portion 65a (*see* Figure 2). *Id.* at col. 6, ll. 61–64. Thereafter, the frequency of signal S12 is divided into signals having ½, ¼, $^1/_8$, and $^1/_{16}$ the frequency of the reference frequency signal S12 as the output signal, as explained above. *Id.* at col. 6, l. 64–col. 7, l. 2. Each output signal having divided frequency is converted logarithmically and becomes logarithmic clock signal TCK, as shown in Figure 4 of Enomoto. *Id.* at col. 7, ll. 2–9.

Logarithmic clock signal TCK generated by logarithmic clock generator 65 is supplied to counter 66, which successively counts counted values 0 to 831. Ex. 1004, col. 7, ll. 17–20. The counted values are sent to input terminal 67a of D/A converter 67. *Id.* at col. 7, ll. 20–21. Converter 67 successively selects output terminals OUT 0 to 9, OUT 10 to 63, and OUT 64 to 831 in accordance with the counted values and then successively turns on switches 67c-1 to 67c-64 through selected output terminals OUT 0 to 9, OUT 10 to 63, and OUT 64 to 831. *Id.* at col. 7, ll. 21–27. Thereby, signal S13 of the voltage, which is set by voltage dividing resistors 67d-1 to 67d-64, is output to output terminal 67b. *Id.* at col. 7. ll. 27–29.

As shown in Figure 3 of Enomoto, D/A converter 67 is provided with a decoder 67c, analog switches 67c-1 to 67c-64, and voltage dividing resisters 67d-1 to 67d-64. Ex. 1004, col 6, ll. 24–29. Decoder 67c is provided with output terminals OUT 0 to 9, OUT 10 to 63, and OUT 64 to 831. *Id.* at col. 6, ll. 29–32. Decoder 67c receives a counted value of counter 66 from input terminal 67a, determines the counted value, and outputs the resultant data. *Id.* at col. 6, ll. 32–35. The output terminal OUT 0 to 9 of decoder 67c outputs a signal S67-1. The output terminal OUT 64 to 831 outputs a signal S67-2. *Id.* at col. 6, ll. 48–50.

We are not persuaded that Enomoto compensates for the acknowledged deficiency in Loke, i.e., the first circuit, pulse counter 30 in Loke, outputting "progressively increasing count values during the accumulating of the count of clock pulses," as required by claims 13 and 37. As described above, in Enomoto, binary counter 65b divides the frequency of the reference frequency signal S12 by 2, 4, 8, and 16. *Id.* at col. 5, ll. 63–64. Clock selection portion 65c selects one of the outputs of counter 65b. *Id.* at col. 5, ll. 65–66. This divided signal is provided to counter 66, which provides an output to D/A converter 67. Decoder 67 receives a counted value of counter 66 from input terminal 67a, determines the counted value, and outputs the resultant data. *Id.* at col. 6, ll. 32–35.

We recognize that counter 66 successively counts counted values 0 to 831, and converter 67 successively selects output terminals OUT 0 to 9, OUT 10 to 63, and OUT 64 to 831 in accordance with the counted values, as explained above. We are not persuaded, however, that this successive counting and selection in Enomoto discloses or suggests progressively increasing count values during the accumulating of the count of clock pulses, as required by the challenged claims. Accordingly, Enomoto does not compensate for the acknowledged deficiencies in Loke.

*c. Articulated Reasoning with Rational Underpinning*

We also are not persuaded that Petitioner has established a reason to combine Loke and Enomoto as proposed regarding the first circuit. Petitioner asserts that it would have been obvious to "modify Loke's interface circuit to include a first circuit that outputs progressively increasing count values during the accumulating of the count of clock pulses as taught by Enomoto. Pet. 16, 39. Petitioner asserts that the proposed combination of Loke and Enomoto "involves no more than a combination of known elements, and the predictable use of such elements according to their established functions to yield predictable results." Pet

16 ( citing Ex. 1008 ¶ 27); *see* Pet. 15 ( citing Ex. 1008 ¶ 26); Pet. 40. According to Petitioner, both Loke and Enomoto employ interface circuits that include counters to accumulate counts of clock pulses. Pet. 16, 40. Petitioner also asserts that both Loke and Enomoto employ D/A converters to transform the outputs of the counters to output signals. *Id.* Based on these assertions, Petitioner concludes that "incorporating the scheme described by Enomoto in a system described by Loke would involve nothing more than common sense or ordinary routine practice of the person of ordinary skill in the art and would facilitate the mapping of intermediate control states, for example to control the brightness of an LED, as taught by Enomoto." *Id.* (citing Ex. 1008 ¶¶ 27, 54).

Exhibit 1008, on which Petitioner relies for evidence, is a declaration by Prasant Mohapatra, Ph.D. Paragraph 26 in Dr. Mohapatra's Declaration is identical to the corresponding text of the Petition, except that Dr. Mohapatra's Declaration adds the phrase "it is my opinion that" immediately before the assertion in the Petition that "a person of ordinary skill in the art would have found it obvious to modify Loke according to the teachings of Enomoto." Ex. 1008 ¶ 26.[3]

Paragraph 27 in Dr. Mohapatra's Declaration also is identical to the corresponding text of the Petition, except that Dr. Mohapatra's Declaration adds the phrase "In my opinion" to the text in the Petition. Ex. 1008 ¶ 27.[4]

Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight. 37 C.F.R. § 42.65(a). Dr. Mohapatra's Declaration does not provide any facts, data, or analysis to

[3] *Compare* Ex. 1008 ¶ 26, *with* Pet. 15, ll. 2–9. We note that the identity between the Declaration and the Petition is not limited to Paragraph 26 of the Declaration. For example, compare paragraphs 18–21 of the Declaration with pages 9–11 of the Petition.

[4] *Compare* Ex. 1008 ¶ 27, *with* Pet. 15–16.

support the opinion stated. Merely repeating an argument from the Petition in the declaration of a proposed expert does not give that argument enhanced probative value. Moreover, Dr. Mohapatra's Declaration does not provide any factual basis for its assertions. The Declaration does not explain the "how," "what," and "why" of the proposed combination of references. Dr. Mohapatra does not explain how the teachings of the specific references could be combined, which combination(s) of elements in specific references would yield a predictable result, or how any specific combination would operate or read on the asserted claims. *ActiveVideo Networks, Inc. v. Verizon Commc'n, Inc*., 694 F.3d 1312, 1327 (Fed. Cir. 2012). Petitioner's and Dr. Mohapatra's statements of general principles from the case law that a proposed combination "involves no more than a combination of known elements," or that a proposed combination is "the predictable use of such elements according to their established functions," or that a proposed combination yields "predictable results" (s*ee* Ex. 1008 ¶ 27) are conclusions; they are not a substitute for a fact-based analysis of the proposed combination of references necessary to support those conclusions. Dr. Mohapatra also fails to explain why a person of ordinary skill in the art would have combined elements from specific references *in the way the claimed invention does. ActiveVideo Networks*, 694 F. 3d at 1328 (citing *KSR Int'l v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)). Accordingly, we give Dr. Mohapatra's Declaration no probative weight.

The existence of common elements found in both the challenged claims and the references relied on by Petitioner (*see* Pet. 16, 40) does not establish that the challenged claims would have been obvious. "[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. "[I]nventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some

sense, is already known." *Id.* at 418–419; *see also Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011) ("Obviousness requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim under examination. Rather, obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention.") (internal citations omitted).

We may not find a patent invalid for obviousness based on "mere conclusory statements." *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) ("However, rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."), *see, KSR*, 550 U.S. 418 (*citing In re Kahn*, 441 F.3d 977). We determine that Petitioner's arguments do not provide the required articulated reasoning with rational underpinning to support the legal conclusion of obviousness.

Based on the analysis above concerning the first circuit, the information presented in the Petition does not show sufficiently that it would have been obvious to combine Loke and Enomoto as proposed by Petitioner to yield the specific invention recited in the challenged claims.

*2. A Second Circuit*

Independent claims 13 and 37 each require a second circuit for mapping the count of encoded clock pulses into a corresponding one of a plurality of control states for the core circuit. Ex. 1001, col. 8, ll. 62–64; col. 11, ll. 34–36. Claims 13 and 37 also each require that the second circuit is responsive to the count values, and operative to map progressively each of the count values output when

accumulating one of a plurality of intermediate control states. *Id.* at col. 4, ll. 6–9; col. 11, ll. 46–49.

The '320 patent discloses that ROM 214 provides a mapping between the EN/SET, or on/off, signal and associated control states for the integrated circuit 200. Ex. 1001, col. 5, ll. 64–65. In some cases, ROM 214 may be replaced with a decoder. *Id.*, col. 6, l. 1.

Petitioner asserts that VCC look-up table 32, Bias look-up table 34, or a combination of the two look-up tables disclosed in Loke is a second circuit for mapping the count of encoded clock pulses into a corresponding one of a plurality of control states for the core circuit. Pet. 11, 40–41. Petitioner acknowledges, however, that "Loke does not explicitly teach the second circuit being 'operative to progressively map each of the count values output during the accumulating to a corresponding one of a plurality of intermediate control states,'" as recited in claims 13 and 37. Pet. 17, 41. Petitioner relies again on Enomoto for the disclosure of this claim limitation. *Id.*

Petitioner again asserts that counter 66 in Enomoto successively counts counted values, which are sent to input terminal 67a of D/A converter 67. *Id.* According to Petitioner, D/A converter 67 successively selects the output terminals in accordance with the counted values and then successively turns on switches through the selected output terminals. *Id.*

As explained above, we are not persuaded that the Enomoto circuit is responsive to the count values, and operative to map progressively each of the count values output when accumulating one of a plurality of intermediate control states, as required by the second circuit in claims 13 and 37.

*a. Articulated Reasoning with Rational Underpinning*

Petitioner asserts that "it would have been obvious for the person of ordinary skill in the art to modify Loke's interface circuit to include a second circuit that

progressively maps each of the count values output during the accumulating to a corresponding one of a plurality of intermediate control states as taught by Enomoto because doing [so] involves no more than a combination of known elements, and the predictable use of such elements according to their established functions to yield predictable results." Pet. 18, 42. Petitioner also argues that the proposed combination would have been obvious because "[b]oth Loke and Enomoto employed interface circuits that included counters to accumulate counts of clock pulses. Further, both employed digital-to-analog (D/A) converters to transform the outputs of the counters to output signals." *Id.* Petitioner concludes, based on these assertions and arguments, that "incorporating the scheme" described by Enomoto "in a system" described by Loke would involve nothing more than common sense or ordinary routine practice of the person of ordinary skill in the art. *Id.* at 42; *see also* Pet. 18. Petitioner also asserts that the proposed modification would facilitate the mapping of intermediate control states, for example, to control the brightness of an LED, as taught by Enomoto. *Id.* at 18 (citing Ex. 1008 ¶ 29). That both the '320 patent and Enomoto are in a "similar field of art" for controlling "luminosity" (Pet. 18–19 (citing Ex. 1008 ¶ 30)) is not persuasive that the specific limitations in claims 13 and 37 would have been obvious based on the specific disclosures in Loke and Enomoto, and the proposed combination of the teachings of these disclosures.

Paragraphs 28, 29, and 30 of Dr. Mohapatra's Declaration essentially are identical to the corresponding text of the Petition.[5] Based on our analysis above, we give Dr. Mohapatra's Declaration no probative weight.

[5] Regarding claim 13, compare pages 16–17 of the Petition with Paragraph 28 of the Declaration; compare pages 17–18 of the Petition with Paragraph 29 of the Declaration; compare pages 18–19 of the Petition with Paragraph 30 of the Declaration. Similarly, regarding claim 37, compare pages 40–43 of the Petition

Our analysis above of the first circuit also is applicable to the second circuit. Accordingly, we determine that Petitioner's arguments do not provide the required articulated reasoning with rational underpinning to support the legal conclusion of obviousness.

Based on the analysis above concerning the second circuit, the information presented in the Petition does not show sufficiently that it would have been obvious to combine Loke and Enomoto as proposed by Petitioner to yield the specific invention recited in the challenged claims.

*3. A Third Circuit*

Independent claim 13 requires a third circuit for resetting the count of encoded clock pulses to zero in response to the received signal being low for a period that exceeds a predetermined timeout value. The predetermined timeout value is longer than a width of one of the encoded clock pulses. Ex. 1001, col. 8, ll. 65–67. Independent claim 37 is similar, but requires a third circuit for resetting the count of encoded clock pulses to zero in response to the received signal being at the first level (rather than "low," as in claim 13). Claim 37 also requires a transition from the second level to the first level after the period that exceeds a predetermined timeout value. *Id.* at col. 11, ll. 37–42.

The '320 patent discloses that "[h]olding the voltage at the EN/SET pin high causes the counter to stop counting and maintain its value. Holding the voltage at the EN/SET pin low for more than a preset timeout period causes the counter to reset to zero." Ex. 1001, col. 2, ll. 6–10. As also explained in the '320 patent, counter 212 resets to zero when sensing circuit 210 transitions the Enable signal to a low value. *Id.* at col. 4, ll. 23–25.

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with Paragraphs 55–57 of the Declaration.

Petitioner acknowledges that "Loke does not explicitly teach 'a third circuit for resetting the count of encoded clock pulses to zero in response to the received signal.'" Pet. 11, 36. Petitioner asserts interdigit timer 13 of Adlhoch discloses the "features" required in the "third circuit" limitations in claims 13 and 37. *Id.* at 12, 36. According to Petitioner, in response to the pulse input being low for an interval greater than the interval between successive pulses of a group (i.e., a period that exceeds a predetermined timeout value), inter-digit timer 13 in Adlhoch produces a pulse to reset pulse counter 11. Pet. 12, 37. Petitioner asserts that "[a] person of ordinary skill in the art would have found it obvious to modify Loke according to the teachings of Adlhoch." *Id.* Petitioner also asserts that the use of signaling schemes in which "an input signal on a serial interface is held low for a period that exceeds a predetermined timeout value longer than a width of an encoded pulse in order to reset a count of the encoded pulses to zero, is a common one – even being used in automotive applications." Pet. 13 (citing Ex. 1005).

Adlhoch discloses a transistorized digital decoder and encoder system. Ex. 1003, col. 1, ll. 43–44. The system in Adlhoch has particular applicability in the context of a dial telephone operation. *Id.* at col. 2, ll. 16–17. Figure 1, reproduced below, shows the basic components of the Adlhoch system.

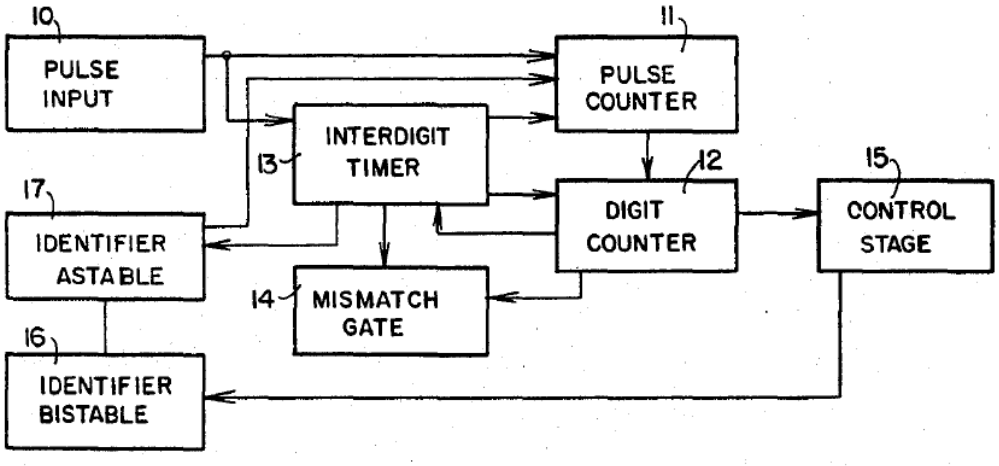


Figure 1 of Adlhoch

Adlhoch discloses pulse input 10 for receiving bursts of tones, such as those transmitted over a radio system, and converting the bursts of tones into direct current pulses. Ex. 1003, col. 2, ll.49–51. Pulses from pulse input 10 are applied to pulse counter 11 and to inter-digit timer 13. *Id.* at col. 2, ll. 52–53. Pulse counter 11 has ten outputs corresponding to the ten possible numbers of each digit. *Id.* at col. 2, ll. 53–55. Inter-digit timer 13 responds to the pulses, and when an interval greater than the interval between successive pulses of a group is received, a pulse is produced and applied to pulse counter 11 to reset. *Id.* at col. 2, ll. 55–58. After the inter-digit interval, the inter-digit timer "relaxes" and applies a pulse to reset the pulse counter and to advance the digit counter to the next stage. *Id.* at col. 3, ll. 35–37. A pulse also is applied to digit counter 12 to actuate the digit counter. *Id.* at col. 2, ll. 59–60. When a match occurs in all stages of digit counter 12, digit counter 12 actuates control stage 15 to actuate a ringing device to indicate that the code number, which is set up, has been received. *Id.* at col. 3, ll. 11–14.

Petitioner asserts it would have been obvious to substitute Loke's "signaling scheme" with Adlhoch's "signaling scheme," because "Loke suggests that signaling schemes other than PDM may be used. Pet. 14 (citing Ex. 1008 ¶ 24). Petitioner also asserts that "[o]ne of ordinary skill in the art would further realize that substituting Loke's signaling scheme with Adlhoch['s] signaling scheme inherently requires the modification of Loke's circuit so that Loke's circuit can accommodate the Adlhoch signaling scheme. Pet. 14 (citing Ex. 1008 ¶ 25).

Petitioner concludes that "one of ordinary skill in the art would realize that the needed modification to Loke's circuit is the addition of Adlhoch's interdigit timer 13," which results in Loke having a third circuit for resetting the count of encoded clock pulses to zero. *Id.* at 14–15 (citing Ex. 1008 ¶ 25).[6]

[6] *See also*, corresponding argument regarding claim 37 on pages 36–39.

As indicated in the analysis above, the rationale for the proposed modification relies on Dr. Mohapatra's Declaration, primarily paragraphs 23–25. Again, the cited paragraphs in the Declaration are identical to the corresponding argument in the Petition.[7] Indeed, both the Petition and the Declaration contain the same error; they both cite to "Ex. 1002 at col. 7, l. 66 - col. 8, l. 18."[8] Exhibit 1002, Loke, however, does not use either column or line numbers. Instead, it uses paragraph numbers to designate its disclosure.

Dr. Mohapatra states the opinion:

> that one of ordinary skill in the art would further realize that substituting Loke's signaling scheme with Adlhoch signaling scheme inherently requires the modification of Loke's circuit so that Loke's circuit can accommodate the Adlhoch signaling scheme (i.e., can receive a sequence of numeric values encoded via bursts of pulses).

Ex. 1008 ¶ 25. Petitioner makes this identical argument. Pet. 14. Neither Dr. Mohapatra nor Petitioner provide a fact-based analysis of why person of ordinary skill would make the proposed realization and substitute Adlhoch's transistorized "signaling scheme" for Loke's "signaling scheme." Moreover, there is no fact-based analysis for what "signaling scheme" in Adlhoch is being substituted into Loke.

Dr. Mohapatra also states the opinion:

> that one of ordinary skill in the art would realize that the needed modification to Loke's circuit is the addition of Adlhoch's interdigit timer 13 (i.e., Adlhoch's interdigit timer 13 would receive as an input Loke's AGC input and produce as an output a signal to reset Loke's pulse counter). The resulting power integrated circuit device of Loke modified by Adlhoch would include "a third circuit for resetting the count of encoded clock pulses to zero.

[7] *E.g.*, *compare* Ex. 1008 ¶ 23, *with* Pet. 12, ll. 3–14.
[8] *See* Pet. 13, 37; Ex. 1008 ¶¶ 23, 51.

Ex. 1008 ¶ 25. Petitioner makes this identical argument. Pet. 14. Neither Dr. Mohapatra nor Petitioner provide a fact-based analysis of why a person or ordinary skill would realize that Loke's circuit needed or would benefit from inter-digit timer 13 disclosed in Adlhoch. This appears to be combination based on hindsight directed by claims 13 and 37 in the '320 patent rather than by the disclosures in the references, market demand, design needs, common sense, or other pertinent factors.

Based on the analysis above concerning the third circuit, the information presented in the Petition does not show sufficiently that it would have been obvious to combine Loke and Adlhoch as proposed by Petitioner to yield the specific invention recited in the challenged claims.

*4. Dependent Claims*

Our analysis above addresses independent claims 13 and 37 and determines, for purposes of this proceeding, that the information in the Petition does not show sufficiently that the first, second, and third circuits would have been obvious based on the cited references. The remaining challenged claims depend from either claim 13 or claim 37. Petitioner does not provide persuasive arguments or evidence directed to the dependent claims that cures the deficiencies discussed above concerning the independent claims.

## III. CONCLUSION

For the foregoing reasons, based on the information presented in the Petition, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in establishing that any of claims 13–24 and 37–47 of the '320 patent are unpatentable based on the proposed combination of Loke, Enomoto, and Adlhoch. Accordingly, we deny the Petition and do not institute an *inter partes* review of claims 13–24 and 37–47 of the '320 patent.

## IV. ORDER

For the reasons given, it is

ORDERED that the Petition is *denied*.

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